

1 1. A lock detection circuit in communication with a phase lock loop to detect
2 phase-frequency lock of an output frequency signal of said phase lock
3 loop with an input reference signal, comprising:

4 a first logic function circuit to combine a frequency increase signal
5 and a frequency decrease signal of said phase lock loop to
6 provide a frequency deviation signal; and

7 a second logic function circuit to combine the frequency deviation
8 signal with the input reference signal to determine that the
9 frequency deviation signal has a greater duration than a portion
10 of a cycle of said input reference signal and provide an error
11 signal.

1 2. The lock detection circuit of claim 1 further comprising a latching circuit in
2 communication with the second logic function and the input reference
3 signal to capture and retain said error signal to provide an unlock alarm
4 signal indicating loss of phase-frequency lock of said phase lock loop.

1 3. The lock detection circuit of claim 1 further comprising an integrator circuit
2 in communication with the second logic function to receive and integrate
3 the error signal and upon the error signal achieving an integrated
4 threshold level, transferring an unlock alarm indicating loss of phase-
5 frequency lock of said phase lock loop.

1 4. The lock detection circuit of claim 1 further comprising a frequency divider
2 connected to receive the input reference signal, divide said input reference
3 signal, and transfer the divided input reference signal to the second
4 function circuit, wherein said second logic function circuit combines the
5 deviation signal and the divided input reference signal to generate the
6 error signal.

1 5. The lock detection circuit of claim 1 wherein the first logic function circuit is
2 an OR gate.

1 6. The lock detection circuit of claim 1 wherein the second logic function
2 circuit is an AND gate.

1 7. A lock detection circuit in communication with a phase lock loop to detect
2 phase-frequency lock of an output frequency signal of said phase lock
3 loop with an input reference signal, comprising:

4 a phase-frequency detector in communication with the phase lock
5 loop to receive the output frequency signal and the input
6 reference signal to generate a frequency increase signal and a
7 frequency decrease signal indicative of an amount of phase-
8 frequency deviation of the output frequency signal has from the
9 input reference signal;

10 a first logic function circuit connected to the phase frequency
11 detector to combine a frequency increase signal and a

12 frequency decrease signal to provide a frequency deviation
13 signal; and
14 a second logic function circuit to combine the frequency deviation
15 signal with the input reference signal to determine that the
16 frequency deviation signal has a greater duration than a portion
17 of a cycle of said input reference signal and provide an error
18 signal.

1 8. The lock detection circuit of claim 7 wherein the first logic function circuit is
2 an OR gate.

1 9. The lock detection circuit of claim 7 wherein the second logic function
2 circuit is an AND gate.

1 10. A phase lock loop system comprising:

2 a phase-frequency detector to detect a difference in frequency
3 between an output frequency of said phase lock loop and an
4 input reference frequency of said phase lock loop; and

5 a lock detection circuit to detect loss of phase-frequency lock of the
6 output frequency signal of said phase lock loop with the input
7 reference signal and upon detection of said loss of phase-
8 frequency lock provide an unlock alarm, said lock detection
9 circuit comprising:

10 a first logic function circuit to combine a frequency increase
11 signal and a frequency decrease signal received from said
12 phase-frequency detector to provide a frequency deviation
13 signal; and
14 a second logic function circuit to combine the frequency
15 deviation signal with the input reference signal to determine
16 that the frequency deviation signal has a greater duration
17 than a portion of a cycle of said input reference signal and
18 provide said unlock alarm.

1 11. The phase lock loop of claim 10 wherein the lock detection circuit further
2 comprises a latching circuit in communication with the second logic
3 function and the input reference signal to capture and retain said unlock
4 alarm to provide an unlock alarm signal indicating loss of phase-frequency
5 lock of said phase lock loop.

1 12. The phase lock loop of claim 10 wherein the lock detection circuit further
2 comprises an integrator circuit in communication with the second logic
3 function to receive and integrate the error signal and upon the error signal
4 achieving an integrated threshold level, transferring an unlock alarm
5 indicating loss of phase-frequency lock of said phase lock loop.

1 13. The phase lock loop of claim 10 wherein the lock detection circuit further
2 comprises a frequency divider connected to receive the input reference

3 signal, divide said input reference signal, and transfer the divided input
4 reference signal to the second function circuit, wherein said second logic
5 function circuit combines the deviation signal and the divided input
6 reference signal to generate the error signal.

7 14. The phase lock loop of claim 10 wherein the first logic function circuit is an
8 OR gate.

1 15. The phase lock loop of claim 10 wherein the second logic function circuit
2 is an AND gate.

1 16. A phase lock loop system comprising:

2 a lock detection circuit to detect loss of phase-frequency lock of an
3 output frequency signal of said phase lock loop with input
4 reference signal and upon detection of said loss of phase-
5 frequency lock provide an unlock alarm, said lock detection
6 circuit comprising:

7 a phase-frequency detector in communication with a voltage
8 controlled oscillator of the phase lock loop to receive the
9 output frequency signal and the input reference signal to
10 generate a frequency increase signal and a frequency
11 decrease signal indicative of an amount of phase-frequency
12 deviation of the output frequency signal has from the input
13 reference signal;

14 a first logic function circuit connected to the phase frequency
15 detector to combine a frequency increase signal and a
16 frequency decrease signal to provide a frequency deviation
17 signal; and

18 a second logic function circuit to combine the frequency
19 deviation signal with the input reference signal to determine
20 that the frequency deviation signal has a greater duration
21 than a portion of a cycle of said input reference signal and
22 provide said unlock alarm.

1 17. The phase lock loop of claim 16 wherein the first logic function circuit is an
2 OR gate.

1 18. The phase lock loop of claim 16 wherein the second logic function circuit
2 is an AND gate.

1 19. A clock extraction circuit to provide an alarm indicating that a local
2 oscillator signal is no longer in phase-frequency synchronism with an
3 reference timing signal extracted from a data stream, said clock extraction
4 circuit comprises:

5 a clock extractor to remove said timing signal from said data
6 stream;

7 a phase lock loop in communication with the clock extractor to
8 receive said timing signal and adjust a phase and frequency of
9 the local oscillator signal synchronize said local oscillator signal
10 to the timing signal; and

11 a lock detection circuit to detect loss of phase-frequency lock of the
12 local oscillator signal with the timing signal and upon detection
13 of said loss of phase-frequency lock provide an unlock alarm,
14 said lock detection circuit comprising:

15 a first logic function circuit to combine a frequency increase
16 signal and a frequency decrease signal received from said
17 phase lock loop to provide a frequency deviation signal, and

18 a second logic function circuit to combine the frequency
19 deviation signal with the timing signal to determine that the
20 frequency deviation signal has a greater duration than a
21 portion of a cycle of said timing signal and provide said
22 unlock alarm.

1 20. The clock extractor of claim 19 wherein the lock detection circuit further
2 comprises a latching circuit in communication with the second logic
3 function and the input reference signal to capture and retain said unlock
4 alarm to provide an unlock alarm signal indicating loss of phase-frequency
5 lock of said phase lock loop.

1 21. The clock extractor of claim 19 wherein the lock detection circuit further
2 comprises an integrator circuit in communication with the second logic
3 function to receive and integrate the error signal and upon the error signal
4 achieving an integrated threshold level, transferring an unlock alarm
5 indicating loss of phase-frequency lock of said phase lock loop.

1 22. The clock extractor of claim 19 wherein the lock detection circuit further
2 comprises a frequency divider connected to receive the input reference
3 signal, divide said input reference signal, and transfer the divided input
4 reference signal to the second function circuit, wherein said second logic
5 function circuit combines the deviation signal and the divided input
6 reference signal to generate the error signal.

7 23. The clock extractor of claim 19 wherein the first logic function circuit is an
8 OR gate.

1 24. The clock extractor of claim 19 wherein the second logic function circuit is
2 an AND gate.

1 25. A clock extraction circuit to provide an alarm indicating that a local
2 oscillator signal is no longer in phase-frequency synchronism with an
3 reference timing signal extracted from a data stream, said clock extraction
4 circuit comprises:

5 a clock extractor to remove said timing signal from said data
6 stream;

7 a phase lock loop in communication with the clock extractor to
8 receive said timing signal and adjust a phase and frequency of
9 the local oscillator signal synchronize said local oscillator signal
10 to the timing signal; and

11 a lock detection circuit to detect loss of phase-frequency lock of the
12 local oscillator signal with the timing signal and upon detection
13 of said loss of phase-frequency lock provide an unlock alarm,
14 said lock detection circuit comprising:

15 a phase-frequency detector in communication with the phase
16 lock loop to receive the output frequency signal and the input
17 reference signal to generate a frequency increase signal and
18 a frequency decrease signal indicative of an amount of
19 phase-frequency deviation of the output frequency signal
20 has from the input reference signal,

21 a first logic function circuit connected to the phase frequency
22 detector to combine a frequency increase signal and a
23 frequency decrease signal to provide a frequency deviation
24 signal, and

25 a second logic function circuit to combine the frequency
26 deviation signal with the timing signal to determine that the
27 frequency deviation signal has a greater duration than a

28 portion of a cycle of said timing signal and provide said
29 unlock alarm.

1 26. The clock extractor of claim 25 wherein the first logic function circuit is an
2 OR gate.

1 27. The clock extractor of claim 25 wherein the second logic function circuit is
2 an AND gate.

3 28. A synchronous communication receiver system to receive a synchronous
4 transport signal containing data and an embedded reference timing signal
5 and to extract said data and the reference timing signal, comprising:

6 a receiver to receive and buffer said synchronous transport signal;
7 and

8 a clock extraction circuit in communication with the receiver to
9 receive the synchronous transport signal and to provide an
10 alarm indicating that a local oscillator signal is no longer in
11 phase-frequency synchronism with an reference timing signal
12 extracted from a data stream, said clock extraction circuit
13 comprises:

14 a clock extractor to remove said timing signal from said
15 synchronous transport signal,

16 a phase lock loop in communication with the clock extractor to
17 receive said reference timing signal and adjust a phase and
18 frequency of the local oscillator signal synchronize said local
19 oscillator signal to the timing signal, and

20 a lock detection circuit to detect loss of phase-frequency lock of
21 the local oscillator signal with the timing signal and upon
22 detection of said loss of phase-frequency lock provide an
23 unlock alarm, said lock detection circuit comprising:

24 a first logic function circuit to combine a frequency increase
25 signal and a frequency decrease signal received from
26 said phase lock loop to provide a frequency deviation
27 signal, and

28 a second logic function circuit to combine the frequency
29 deviation signal with the timing signal to determine that
30 the frequency deviation signal has a greater duration
31 than a portion of a cycle of said timing signal and provide
32 said unlock alarm.

1 29. The synchronous communication receiver system of claim 28 wherein the
2 lock detection circuit further comprises a latching circuit in communication
3 with the second logic function and the input reference signal to capture

4 and retain said unlock alarm to provide an unlock alarm signal indicating
5 loss of phase-frequency lock of said phase lock loop.

1 30. The synchronous communication receiver system of claim 28 wherein the
2 lock detection circuit further comprises an integrator circuit in
3 communication with the second logic function to receive and integrate the
4 error signal and upon the error signal achieving an integrated threshold
5 level, transferring an unlock alarm indicating loss of phase-frequency lock
6 of said phase lock loop.

1 31. The synchronous communication receiver system of claim 28 wherein the
2 lock detection circuit further comprises a frequency divider connected to
3 receive the input reference signal, divide said input reference signal, and
4 transfer the divided input reference signal to the second function circuit,
5 wherein said second logic function circuit combines the deviation signal
6 and the divided input reference signal to generate the error signal.

1 32. The synchronous communication receiver system of claim 28 wherein the
2 first logic function circuit is an OR gate.

1 33. The synchronous communication receiver system of claim 28 wherein the
2 second logic function circuit is an AND gate.

1 34. A synchronous communication receiver system to receive a synchronous
2 transport signal containing data and an embedded reference timing signal
3 and to extract said data and the reference timing signal, comprising:

4 a receiver to receive and buffer said synchronous transport signal;
5 and

6 a clock extraction circuit in communication with the receiver to
7 receive the synchronous transport signal and to provide an
8 alarm indicating that a local oscillator signal is no longer in
9 phase-frequency synchronism with an reference timing signal
10 extracted from a data stream, said clock extraction circuit
11 comprises:

12 a clock extractor to remove said timing signal from said
13 synchronous transport signal,

14 a phase lock loop in communication with the clock extractor to
15 receive said reference timing signal and adjust a phase and
16 frequency of the local oscillator signal synchronize said local
17 oscillator signal to the timing signal, and

18 a lock detection circuit to detect loss of phase-frequency lock of
19 the local oscillator signal with the timing signal and upon
20 detection of said loss of phase-frequency lock provide an
21 unlock alarm, said lock detection circuit comprising:

22 a phase-frequency detector in communication with the phase
23 lock loop to receive the output frequency signal and the
24 input reference signal to generate a frequency increase

25 signal and a frequency decrease signal indicative of an
26 amount of phase-frequency deviation of the output
27 frequency signal has from the input reference signal,
28 a first logic function circuit connected to the phase frequency
29 detector to combine a frequency increase signal and a
30 frequency decrease signal to provide a frequency
31 deviation signal, and
32 a second logic function circuit to combine the frequency
33 deviation signal with the timing signal to determine that
34 the frequency deviation signal has a greater duration
35 than a portion of a cycle of said timing signal and provide
36 said unlock alarm.

1 35. The clock extractor of claim 34 wherein the first logic function circuit is an
2 OR gate.

1 36. The clock extractor of claim 34 wherein the second logic function circuit is
2 an AND gate.

1 37. A synchronous communication system for the transfer of a synchronous
2 transport signal, comprising:

3 a synchronous transmission apparatus to combine a data signal
4 and a timing reference signal to form the synchronous transport
5 signal; and

6 a synchronous communication receiver apparatus in
7 communication with the synchronous transmission apparatus to
8 receive the synchronous transport signal band to extract said
9 data and the reference timing signal, comprising:

10 a receiver to receive and buffer said synchronous transport
11 signal,

12 a clock extraction circuit in communication with the receiver to
13 receive the synchronous transport signal and to provide an
14 alarm indicating that a local oscillator signal is no longer in
15 phase-frequency synchronism with the reference timing
16 signal extracted from a synchronous transport signal, said
17 clock extraction circuit comprises:

18 a clock extractor to remove said timing signal from said
19 synchronous transport signal,

20 a phase lock loop in communication with the clock extractor
21 to receive said reference timing signal and adjust a
22 phase and frequency of the local oscillator signal

synchronize said local oscillator signal to the timing
signal, and

a lock detection circuit to detect loss of phase-frequency lock
of the local oscillator signal with the timing signal and
upon detection of said loss of phase-frequency lock
provide an unlock alarm, said lock detection circuit
comprising:

a first logic function circuit to combine a frequency
increase signal and a frequency decrease signal
received from said phase lock loop to provide a
frequency deviation signal, and

a second logic function circuit to combine the frequency
deviation signal with the timing signal to determine
that the frequency deviation signal has a greater
duration than a portion of a cycle of said timing signal
and provide said unlock alarm.

38. The synchronous communication system of claim 37 wherein the lock
detection circuit further comprises a latching circuit in communication with
the second logic function and the input reference signal to capture and
retain said unlock alarm to provide an unlock alarm signal indicating loss
of phase-frequency lock of said phase lock loop.

1 39. The synchronous communication system of claim 37 wherein the lock
2 detection circuit further comprises an integrator circuit in communication
3 with the second logic function to receive and integrate the error signal and
4 upon the error signal achieving an integrated threshold level, transferring
5 an unlock alarm indicating loss of phase-frequency lock of said phase lock
6 loop.

1 40. The synchronous communication system of claim 37 wherein the lock
2 detection circuit further comprises a frequency divider connected to
3 receive the input reference signal, divide said input reference signal, and
4 transfer the divided input reference signal to the second function circuit,
5 wherein said second logic function circuit combines the deviation signal
6 and the divided input reference signal to generate the error signal.

7 41. The synchronous communication system of claim 37 wherein the first logic
8 function circuit is an OR gate.

1 42. The synchronous communication system of claim 37 wherein the second
2 logic function circuit is an AND gate.

1 43. The synchronous communication system of claim 37 wherein said
2 synchronous communication system is a SONET communication system.

1 44. A synchronous communication system for the transfer of a synchronous
2 transport signal, comprising:

3 a synchronous transmission apparatus to combine a data signal
4 and a timing reference signal to form the synchronous transport
5 signal;

6 a synchronous communication receiver apparatus in
7 communication with the synchronous transmission apparatus to
8 receive the synchronous transport signal band to extract said
9 data and the reference timing signal, comprising:

10 a receiver to receive and buffer said synchronous transport
11 signal,

12 a clock extraction circuit in communication with the receiver to
13 receive the synchronous transport signal and to provide an
14 alarm indicating that a local oscillator signal is no longer in
15 phase-frequency synchronism with the reference timing
16 signal extracted from a synchronous transport signal, said
17 clock extraction circuit comprises:

18 a clock extractor to remove said timing signal from said
19 synchronous transport signal,

20 a phase lock loop in communication with the clock extractor
21 to receive said reference timing signal and adjust a
22 phase and frequency of the local oscillator signal

23 synchronize said local oscillator signal to the timing
24 signal, and

25 a lock detection circuit to detect loss of phase-frequency lock
26 of the local oscillator signal with the timing signal and
27 upon detection of said loss of phase-frequency lock
28 provide an unlock alarm, said lock detection circuit
29 comprising:

30 a phase-frequency detector in communication with the
31 phase lock loop to receive the output frequency signal
32 and the input reference signal to generate a
33 frequency increase signal and a frequency decrease
34 signal indicative of an amount of phase-frequency
35 deviation of the output frequency signal has from the
36 input reference signal,

37 a first logic function circuit connected to the phase
38 frequency detector to combine a frequency increase
39 signal and a frequency decrease signal to provide a
40 frequency deviation signal, and

41 a second logic function circuit to combine the frequency
42 deviation signal with the timing signal to determine
43 that the frequency deviation signal has a greater

44 duration than a portion of a cycle of said timing signal
45 and provide said unlock alarm.

1 45. The synchronous communication system of claim 44 wherein the first logic
2 function circuit is an OR gate.

1 46. The synchronous communication system of claim 44 wherein the second
2 logic function circuit is an AND gate.

1 47. The synchronous communication system of claim 44 wherein said
2 synchronous communication system is a SONET communication system.

1 48. A method for providing an unlock alarm denoting loss of phase frequency
2 synchronism of a phase lock loop comprising the steps of:

3 providing an input reference timing signal;

4 providing an increase frequency signal and a decrease frequency
5 signal from said phase lock loop said increase and decrease
6 frequency signals indicating existence of an error in the phase-
7 frequency between an input reference timing signal applied to
8 said phase lock loop and an output local oscillator signal;

9 performing a first logical combining of said increase frequency
10 signal and said decrease frequency signal to create a phase-
11 frequency deviation signal;

performing a second logical combining of said phase-frequency deviation signal and the input reference timing signal;

if the phase-frequency deviation signal has a greater duration than a portion of a cycle of said timing signal, providing the unlock alarm signal.

49. The method of claim 48 further comprising the step of:

capturing and retaining said unlock alarm signal for transfer to external circuitry.

50. The method of claim 48 further comprising the steps of:

integrating the unlock alarm signal; and

upon said integrated unlock alarm signal surpassing a threshold value transferring externally said unlock alarm signal.

51. The method of claim 48 further comprising the step of:

dividing the input reference timing signal; and

performing the second logical combining the phase-frequency error signal and the divided input reference timing signal.

52. The method of claim 48 wherein the first logical combining is an OR function.

1 53. The method of claim 48 wherein the second logic logical combining is an
2 AND function.

1 54. A method for providing an unlock alarm denoting loss of phase frequency
2 synchronism of a phase lock loop comprising the steps of:

3 providing an input reference timing signal;

4 providing an output timing signal from said phase lock loop;

5 detecting a phase-phase frequency deviation between the output
6 timing signal and the input reference timing signal;

7 if said output timing signal lags or has a lower frequency than said
8 input reference timing signal providing an increase frequency
9 signal;

10 if said output timing signal leads or has a higher frequency than
11 said input reference timing signal providing a decrease
12 frequency signal;

13 performing a first logical combining of said increase frequency
14 signal and said decrease frequency signal to create a phase-
15 frequency deviation signal;

16 performing a second logical combining of said phase-frequency
17 deviation signal and the input reference timing signal;

18 if the phase-frequency deviation signal has a greater duration than
19 a portion of a cycle of said timing signal, providing the unlock
20 alarm signal.

21 55. The method of claim 54 wherein the first logical combining is an OR
22 function.

1 56. The method of claim 54 wherein the second logic logical combining is an
2 AND function.